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10/614,558	07/07/2003	David E. Jones	2037.1010-002	5801

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EXAMINER	
FOUD, HICHAM B	
ART UNIT	**PAPER NUMBER**
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/614,558	JONES, DAVID E.	
	Examiner	Art Unit	
	Hicham B. Foud	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/07/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, 17, 18, 25, and 31 of U.S. Patent No. 6,590,901. Although the conflicting claims are not identical, they are not patentably distinct from each other because.

For claims 1 and 2, claim 3 of U.S. Patent No. 6,590,901 discloses a packet buffer random access memory (PBRAM) device, comprising: (a) a memory array; (b) a plurality of input and output ports to be coupled to a network controller device; (c) a plurality of serial registers associated with the input and output ports, the serial registers simultaneously receiving packet data from the input ports and writing packet data to the memory array, the serial registers further being segmented into a plurality of segments, segments of respective serial registers being associated with corresponding portions of the memory array, segments of different serial registers simultaneously transferring packet data to different portions of the memory array, packet data is transferred into one segment of a serial register as data is simultaneously transferred out of another segment of the serial register; (d) a plurality of command control units each for receiving a command that indicates a selected operation to be performed by the PBRAM device;

and (e) a memory management device for determining a location in the memory array where the packet data is to be written, that determination being made in response to a command that indicates that a write operation is to be performed.

Claims 1 and 2 of the instant application merely broadens the scope of the claim 3 of the Patent (U.S. Patent No. 6,590,901) by eliminating the elements (d) and (e) and their functions of the claims. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

For claim 7, claim 18 of U.S. Patent No. 6,590,901 discloses a method for storing data packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising the steps of: receiving a plurality of data packets from controllers coupled to the computer network at a plurality of input ports of the PBRAM device; serially transferring portions of the data packets to different segments of serial registers that are connected between the input ports and a memory array; conveying the portions of the data packets to the memory array portion of the PBRAM device in parallel, while concurrently transferring other portions of the packets to other segments of the serial registers; storing pointers to the packets in a packet table portion of the memory array; assigning input queue structures, contained in a memory array portion of the PBRAM device; and storing pointers to associated locations of the packet table in the queue structures, the queue structures being further accessible by a

plurality of output ports of the PBRAM device such that the pointers are transferred from the input queue structures to associated output queue structures that deliver the data packets to associated output ports.

Claim 7 of the instant application merely broadens the scope of the claim 18 of the Patent (U.S. Patent No. 6,590,901) by eliminating the elements (storing pointers to the packets in a packet table portion of the memory array; assigning input queue structures, contained in a memory array portion of the PBRAM device; and storing pointers to associated locations of the packet table in the queue structures, the queue structures being further accessible by a plurality of output ports of the PBRAM device such that the pointers are transferred from the input queue structures to associated output queue structures that deliver the data packets to associated output ports) and their functions of the claims. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

For claims 12, claim 25 of U.S. Patent No. 6,590,901 discloses a packet buffer random access memory (PBRAM) device comprising: a memory array; a plurality of input and output ports coupled to the memory array by serial registers for conveying data to and from the memory array; a plurality of command ports for receiving commands that indicate desired operations to be performed in relation to the data conveyed on the input and output ports; a memory management unit coupled between

the control ports and the memory array, the memory management unit establishing input queue structures within the memory array responsive to write commands issued on the command ports, the input queue structures for receiving pointers to locations in a packet table that point to the data that is conveyed from the input ports, the memory management device is incorporated on the same semiconductor chip as the PBRAM device

Claim 12 of the instant application merely broadens the scope of the claim 25 of the Patent (U.S. Patent No. 6,590,901) by eliminating the elements (the memory management device is incorporated on the same semiconductor chip as the PBRAM device) and their functions of the claims. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

For claim 14, claim 31 of U.S. Patent No. 6,590,901 discloses a method for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising the steps of: receiving a packet from a controller coupled to the computer network by one of a plurality of input ports of the PBRAM device; storing the packet in a physical location of a memory array of the PBRAM device; storing a pointer to the physical location in an entry of a packet table in the memory array; storing a pointer to the entry in the packet table in an input queue structure, contained in a memory array portion of the PBRAM device; the input queue

structure being further accessible by a plurality of output ports of the PBRAM device such that the pointer in the input queue structure is transferred to an associated output queue structure; asserting, by the controller, a plurality of data elements that comprise the packet on a data signal associated with the input port; causing a clock signal associated with the input port to oscillate at a frequency synchronous to the assertion of the plurality of data elements; and asserting a mask signal associated with the input port in synchronization with associated ones of the plurality of data elements such that a meaning of each data element is qualified, the qualification indicating the data element contains a valid logic level, the data element does not contain a valid logic level or that the data element indicates that it is the last data element of the packet.

Claim 14 of the instant application merely broadens the scope of the claim 31 of the Patent (U.S. Patent No. 6,590,901) by eliminating the elements (asserting, by the controller, a plurality of data elements that comprise the packet on a data signal associated with the input port; causing a clock signal associated with the input port to oscillate at a frequency synchronous to the assertion of the plurality of data elements; and asserting a mask signal associated with the input port in synchronization with associated ones of the plurality of data elements such that a meaning of each data element is qualified, the qualification indicating the data element contains a valid logic level, the data element does not contain a valid logic level or that the data element indicates that it is the last data element of the packet) and their functions of the claims. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*,

136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

For claim 18, claim 1 of U.S. Patent No. 6,590,901 discloses an apparatus for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising: means for receiving a plurality of packets from controllers coupled to the computer network by a plurality of input ports of the PBRAM device; means for assigning input queue structures, contained in a memory array portion of the PBRAM device, to store packets; means for serially transferring portions of the packets to different segments of serial registers that are connected to the input ports and to the memory array; means for conveying the portions of the packets to the memory array portion of the PBRAM device in parallel; means for storing the packets in the queue structures, the queue structures being further accessible by a plurality of output ports of the PBRAM device such that the input queue structures become output queue structures that deliver the packets to associated output ports; means for asserting a plurality of data elements that comprise each of the packets on data signals that are associated with the input ports; means for causing clock signals, that are associated with the input ports, to oscillate at frequencies indicating when each of the plurality of data elements are valid; and means for asserting mask signals, associated with each of the input ports, in synchronization with associated ones of the plurality of data elements such that a meaning of each data element is qualified, the

qualification indicating the data element either contains a valid logic level, does not contain a valid logic level or is the last data element of the associated packet.

Claim 18 of the instant application merely broadens the scope of the claim 1 of the Patent (U.S. Patent No. 6,590,901) by eliminating the elements (means for asserting a plurality of data elements that comprise each of the packets on data signals that are associated with the input ports; means for causing clock signals, that are associated with the input ports, to oscillate at frequencies indicating when each of the plurality of data elements are valid; and means for asserting mask signals, associated with each of the input ports, in synchronization with associated ones of the plurality of data elements such that a meaning of each data element is qualified, the qualification indicating the data element either contains a valid logic level, does not contain a valid logic level or is the last data element of the associated packet.) and their functions of the claims. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

For claim 22, claim 17 of U.S. Patent No. 6,590,901 discloses an apparatus for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising: means for receiving a packet from a controller coupled to the computer network by one of a plurality of input ports of the PBRAM device, the means for receiving further comprising: means for asserting, by the

controller, a plurality of data elements that comprise the packet on a data signal associated with the input port; means for causing a clock signal associated with the input port to oscillate at a frequency indicating when each of the plurality of data elements are valid; and means for asserting a mask signal associated with the input port in synchronization with associated ones of the plurality of data elements such that a meaning of each data element is qualified, the qualification indicating the data element contains a valid logic level, the data element does not contain a valid logic level or that the data element indicates that it is the last data element of the packet; means for assigning an input queue structure, contained in a memory array portion of the PBRAM device, to store the packet, the memory array being shared by the plurality of input ports; and means for storing the packet in the queue structure, the queue structure being further accessible by a plurality of output ports of the PBRAM device such that the input queue structure becomes an output queue structure that delivers the packet to an associated output port.

Claim 22 of the instant application merely broadens the scope of the claim 17 of the Patent (U.S. Patent No. 6,590,901) by eliminating the elements (the means for receiving further comprising: means for asserting, by the controller, a plurality of data elements that comprise the packet on a data signal associated with the input port; means for causing a clock signal associated with the input port to oscillate at a frequency indicating when each of the plurality of data elements are valid; and means for asserting a mask signal associated with the input port in synchronization with associated ones of the plurality of data elements such that a meaning of each data

element is qualified, the qualification indicating the data element contains a valid logic level, the data element does not contain a valid logic level or that the data element indicates that it is the last data element of the packet) and their functions of the claims. It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

For claims 3-6, 8-11, 13, 15-17, 19-21 and 23-25 are rejected because it would have been obvious over the claims of the U.S. Patent No. 6,590,901 to have a portion of the memory array as a queue, wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level, wherein packet data is read from the sub-queue with the highest priority level that stores data and wherein the memory array is a single global memory. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to have a portion of the memory array as a queue, wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level, wherein packet data is read from the sub-queue with the highest priority level that stores data and wherein the memory array is a single global memory. The motivation of having a portion of the memory array as a queue, wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level, wherein packet data is read from the sub-queue with the highest priority level that stores data and wherein the memory array is a single global memory is being that is gives a good

arrangement to the memory for easier function by dividing a queue to a plurality of sub-queues, organize the reading/writing of packet data by assigning a priority level to the correspondent subqueues to reduce the memory latency and allowing all the stored data in the memory available to all the ports by having a single global memory.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12, 13 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 12 line 8, the term "the control ports" has no antecedent basis.

In claim 16 line 8 and 9 respectively, the terms "the sub-queue" and "the highest priority level" have no antecedent basis.

Claim 13 is rejected because it depends on the rejected claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7, 12, 14, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Toda et al (5,612,925).

For claim 1, Toda et al discloses a packet buffer random access memory (PBRAM) device, comprising: (a) a memory array (see figure 16 element 162 wherein the is arranged by cell group); (b) a plurality of input and output ports to be coupled to a network controller device (see Figure 16 element 164, I/O section is coupled to a control section which is element 166), the memory array for storing packet data received by the plurality of input ports being shared by the plurality of input and output ports (see figure 16, element 164 wherein data is shared by I/O); and (c) a plurality of serial registers associated with the input and output ports (see Figure 16 element 164 is connected to I/O), the serial registers simultaneously receiving packet data from the input ports and writing packet data to the memory array (see Figure 16, wherein the connection between the I/O and serial registers and the memory cell group), the serial registers further being segmented into a plurality of segments, segments of respective serial registers being associated with corresponding portions of the memory array(see Figure 16 wherein the section 164 is segmented to a plurality of segments that are associated to a corresponding memory cell group), segments of different serial registers simultaneously transferring packet data to different portions of the memory array (see column 12 lines 8-12).

For claim 2, Toda et al discloses a packet buffer random access memory (PBRAM) device wherein packet data is transferred into one segment of a serial register as data is simultaneously transferred out of another segment of the serial register (see Figure 16, the connection between the I/O, serial registers and the memory and see column 12 lines 8-12).

Claim 7 is rejected for same reasons as claim 1, since claim 7 is the method carried out by the system of claim 1.

For claim 12, Toda et al discloses a packet buffer random access memory (PBRAM) device comprising: a memory array (see figure 16 element 162 wherein the is arranged by cell group); a plurality of input and output ports coupled to the memory array by serial registers for conveying data to and from the memory array (see Figure 16 element 164 is connected to I/O which is element 164), the memory array for storing packet data received by the plurality of ports being shared by the plurality of input and output ports (see Figure 16, wherein the connection between the I/O and serial registers and the memory cell group); a plurality of command ports for receiving commands that indicate desired operations to be performed in relation to the data conveyed on the input and output ports (see Figure 16, wherein the element 166 which is control section send commands to the data section to perform the desired operations); and a memory management unit coupled between the control ports and the memory array (see Figure 16, elements 163, 168 and 165), the memory management unit establishing input queue structures within the memory array responsive to write commands issued on the command ports (see figure 16, wherein element 163 is connected to the control section 166), the input queue structures for receiving pointers to locations in a packet table that point to the data that is conveyed from the input ports (see figure 16, element 163 which comprises of addresses of the data in the memory and designates the memory cells which are to be accessed (see column 5 lines 11-15)).

For claim 14, Toda et al discloses a method for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising the steps of: receiving a packet from a controller coupled to the computer network by one of a plurality of input ports of the PBRAM device (see figure 16, element 164 wherein data is shared by I/O); storing the packet in a physical location of a memory array of the PBRAM device (see figure 16, element 162 wherein data is stored), the memory array being shared by the plurality of input ports (see figure 16, element 164 wherein data is shared by I/O); storing a pointer to the physical location in an entry of a packet table in the memory array (see figure 16, element 162 wherein data is stored); storing a pointer to the entry in the packet table in an input queue structure, contained in the memory array of the PBRAM device (see figure 16, element 163 which comprises addresses of the data in the memory and designates the memory cells which are to be accessed (see column 5 lines 11-15)); and the input queue structure being further accessible by a plurality of output ports of the PBRAM device such that the pointer in the input queue structure is transferred to an associated output queue structure (see Figure 16 wherein element 163 is connected to I/O (element 164) through the control section (element 166) and the addresses of the data stored in the memory is inherent to the pointers are in the element 163 which is considered both input and output queue).

For claim 18 and 22 are rejected for same reasons as claims 7 and 14, since claims 18 and 22 are the apparatus carried out by the method of claim 7 and 14.

Claim Rejections - 35 USC § 103

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 11, 13, 17, 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda et al.

For claims 6, 11, 13, 17, 21 and 25 are rejected because it would have been obvious over the claimed invention of Toda et al to have the memory array as a single global memory. The difference between the memory array as taught by the invention of Toda et al and the single global memory is that the memory array is a specific arrangement of memory that can be depending on different factors such as data type, and the single global memory is a regular memory that holds all data without any specific arrangement. Therefore, an official notice is taken in that a memory array can be arranged as a single global memory. Thus, it would have been obvious to the

person of ordinary skill in the art at the time of the invention to have the memory array as a single global memory. The motivation of having the memory array as a single global memory is being that it allows all the stored data in the memory available to all the ports and for simplicity.

8. Claims 3-5, 8-10, 15, 16, 19, 20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda et al in view of Zuravleff et al (5,867,735).

For claims 3-5, 8-10, 15,16, 19, 20, 23 and 24, Toda et al discloses all the subject matter with the exception of wherein a portion of the memory array is a queue, the queue includes a plurality of sub-queues and each sub-queue assigned a priority level wherein packet data is read from the sub-queue with the highest priority level that stores data. However, the invention of Zuravleff et al from the same or similar fields of endeavor shows that a portion of the memory array is a queue (see column 6 lines 65-66, wherein elements 114 are queues), the queue includes a plurality of sub-queues (see column 10 lines 25-27, wherein elements 114 are divided to elements 214 which are subqueues) and each sub-queue assigned a priority level (see column 10 lines 31-32 wherein each subqueue has a unique priority level) wherein packet data is read from the sub-queue with the highest priority level that stores data (see column 10 lines 39-42 wherein the highest priority level subqueues are read first). Thus, it would have been obvious to the person of ordinary skill in the art at the time of invention to use the division of queues to subqueues and the method of priority level of subqueues as taught by the invention of Zuravleff et al in the invention of Toda et al. The motivation of having a portion of the memory array as a queue, wherein the queue includes a plurality

of sub-queues, each sub-queue assigned a priority level and wherein packet data is read from the sub-queue with the highest priority level that stores data is being that is gives a good arrangement to the memory for easier function by dividing a queue to a plurality of sub-queues, and read the packet data that were stored in subqueues which are assigned a highest priority level to them before any other subqueues to reduce the effect of memory latency.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ikeda (5,703,822), Pinkham et al (4,891,795), Yamaguchi et al (4,947,373) and Toda et al (5,875,486) are cited to show a system that is considered pertinent to the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hicham B. Foud whose telephone number is 571-270-1463. The examiner can normally be reached on Monday - Thursday 10-3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hicham Foud

HF

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600